REMARKS

Claims 1 - 6 and 12 - 15 have been canceled without prejudice or disclaimer.

Claims 7 - 10 and 16, 17, 19 and 20 have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicants regard as their invention. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated October 23, 2003.

Claims 7 – 11 and 16 - 20 are presently being examined.

Claim 16 is rejected under 35 USC §112, second paragraph, for the specific reason set forth on page 2 of the outstanding Action. Here, the Examiner states that it is not understood how the first and second buried layers form a PN junction to the first and second buried layers, respectively.

The applicants respectfully request reconsideration of this rejection.

In response, the language in claim 6 (i.e., "first and second buried layers") in question has been changed to "first and second base layers."

Also, in order to more particularly point out and distinctly claim the subject matter to which the applicants are entitled, claims 7 - 10, 17, 19 and 20 have been amended in order to correct certain informalities therein.

Accordingly, the withdrawal of the outstanding indefiniteness rejection under 35 USC §112, second paragraph, is in order, and is therefore respectfully solicited.

As to the merits of this case, the following outstanding obviousness rejections under 35 USC §103 are discussed below.

First, claims 7 - 9 are rejected under 35 USC §103(a) based on Webb (U.S. Patent No. 5,516,705). The applicants respectfully request reconsideration of this rejection.

In response to the Examiner's position with respect to Webb, as set forth in line 1, page 3 through line 6, page 4 of the outstanding Action, the applicants respectfully submit that the PN junctions between base layers and buried layers are not taught by Webb to be planar.

Furthermore, Webb teaches away from making the PN junction between base layers and buried layers planar in order to reduce the overshoot voltage. That is, Webb teaches that having multiple buried regions (42), which are substantially aligned with "dot" regions (37), reduces the overshoot voltage. However, multiple buried regions do not form a planar PN junction.

Additionally, the applicants have amended claim 7 in order to specifically recite that the PN junctions between the base layers and the buried layers are planar so as to more clearly define the claimed invention.

As to the claimed method of claim 8, Webb (at col. 9, lines 39 - 43) teaches the use of windows for forming the buried layers. The "completely exposed" method of present claim 8 is distinct from a "windows" method.

The applicants further respectfully refer the Examiner to lines 17 - 21, page 3 of the applicants' specification, which summarily state that the applicants' claimed invention: "sets out to resolve the problems encountered in the related art[; i.e.,] it is the object of the present invention to provide a surge protection semiconductor device that has a straightforward manufacturing process, a simple structure, and is highly reliable." The applicants respectfully submit that the claimed method and the above-mentioned benefit or advantage derived therefrom are not taught by the cited prior art.

Accordingly, a person of ordinary skill in the art would not have found the applicants' claimed invention obvious under 35 USC §103(a) based on Webb; and the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Webb (U.S. Patent No. 5,516,705) is in order, and is therefore respectfully solicited.

Secondly, claims 10, 16 and 17 are rejected under 35 USC §103(a) based on Webb, and further in view of Takizawa (U.S. Patent No. 5,962,878) and Assour (U.S. Patent No. 4,292,646).

The Examiner alleges that Webb teaches the applicants' invention recited in claims 7 - 9, but does not teach ring-shaped moats; and that Takizawa teaches moats (16) with bottom surfaces reaching the buried layers (46); and further that Assour teaches a ring-shaped moat (69).

The applicants respectfully request reconsideration of this rejection.

The lack of the teaching of planar PN junctions in the Webb reference is discussed above. As to the secondary reference of Takizawa, component (16) of the semiconductor of Takizawa is described as being an "emitter-push restraining layer." The purpose of the emitter-push restraining layer is to remove the stage differences at end portions of the diffusion layers. The emitter-push restraining layer is made up of a P-type material as opposed to an oxide, such as silicon oxide, found in the present moats.

The emitter-push restraining layers (16) are higher in impurity concentration than the base layer (20); and that they are formed before forming the base layer (20), as described at col. 11, line 60 to col. 12, line 35 of Takizawa. The emitter-push restraining layers are formed by diffusing the impurities into the substrate surface. A layer formed in such a manner would not be a "moat" as is described and defined in the present application, and as is known in the art. A moat is presently described as being formed by removing material, such as by etching.

Additionally, Takizawa's method teaches away from the method for providing a planar PN junction as the presence of the emitter-push restraining layers (16) during the present diffusing step for the buried layers would certainly not promote a planar junction, as obtained by using the present "completely exposed" method.

Regarding the other secondary reference of Assour, component (69) of the semiconductor of Assour is described as being an "isolation moat." The moat (69) is filled with a dielectric material and laterally isolates a gate trigger region (68) from adjacent regions of the semiconductor. Assour is relied on solely for teaching a "moat," which is not presently claimed to be novel. Assour, in any event, does not teach or suggest the present feature of providing planar PN junctions and the use of moats to obtain the planar PN junctions.

In view of the above, even if, *arguendo*, the teachings Webb, Takizawa and Assour can be combined in the manner suggested by the Examiner, such combined teachings would still fall far short in fully meeting the applicants' claimed invention. As such, a person of ordinary skill in the art would not have found the applicants' claimed invention obvious under 35 USC §103(a) based on Webb, Takizawa and Assour, singly or in combination.

Accordingly, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Webb, and further in view of Takizawa (U.S. Patent No. 5,962,878) and Assour (U.S. Patent No. 4,292,646) is in order, and is therefore respectfully solicited.

Thirdly, claims 11 and 18 are rejected under 35 USC §103(a) based on Webb, Takizawa and Assour, and further in view of Planey (U.S. Patent No. 3,772,577).

The Examiner alleges that Webb, Takizawa and Assour teach the claimed features of the applicants' claimed invention, but do not teach insides of moats filled with oxide. The Examiner further alleges that Planey teaches moats (12) filled with oxide (Fig. 3 and col. 2, lines 30 - 51).

The applicants respectfully request reconsideration of this rejection.

The applicants take the position that Planey does not supplement the above-discussed deficiencies of the other cited references. That is, the applicants traverse this rejection based on claim 11 depending from claim 7, and claim 18 depending from claim 16; and that the applicants' above comments with respect to claims 7 and 16 are similarly applicable here.

Accordingly, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Webb, Takizawa and Assour, and further in view of Planey (U.S. Patent No. 3,772,577) is in order, and is therefore respectfully solicited.

Lastly, claims 5, 19 and 20 are rejected under 35 USC §103(a) based on Webb, Takizawa and Assour, and further in view of Casey (U.S. Patent No. 6,448,589).

Claim 5 is a canceled claim; thus, the rejection of claim 5 is moot.

As to claims 19 and 20, the Examiner alleges that Casey teaches at least part of the base layers (48) and (49) positioned at a region or exposed at a surface on the outside of the or a region located at an outer periphery of the moats (76) and (79) of the surface of the semiconductor substrate (42) and (66), and at least a part of the first and second buried layers (56) and (57) are exposed at a surface of a region located at an outer periphery of the first and second moats ("Figure 2, col. 4-6, all lines").

The applicants respectfully request reconsideration of this rejection.

The applicants respectfully submit that at least a part of the buried layers (56) and (57) are not exposed as alleged.

Casey is relied on solely for teaching the exposed layers; and does not supplement the above-discussed deficiencies of the other references.

Accordingly, the applicants respectfully traverse the rejection of claims 19 and 20 based on their dependencies from claim 16; and that the applicants' above comments with respect to claim 16 are similarly applicable here.

Additionally, with respect to claim 20, the applicants respectfully traverse its rejection based on the fact that it lacks any teaching of exposed buried layers, as discussed above.

Accordingly, the withdrawal of the outstanding obviousness rejection under 35 USC §103(a) based on Webb, Takizawa and Assour, and further in view of Casey (U.S. Patent No. 6,448,589) is in order, and is therefore respectfully solicited.

In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact the applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, the applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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